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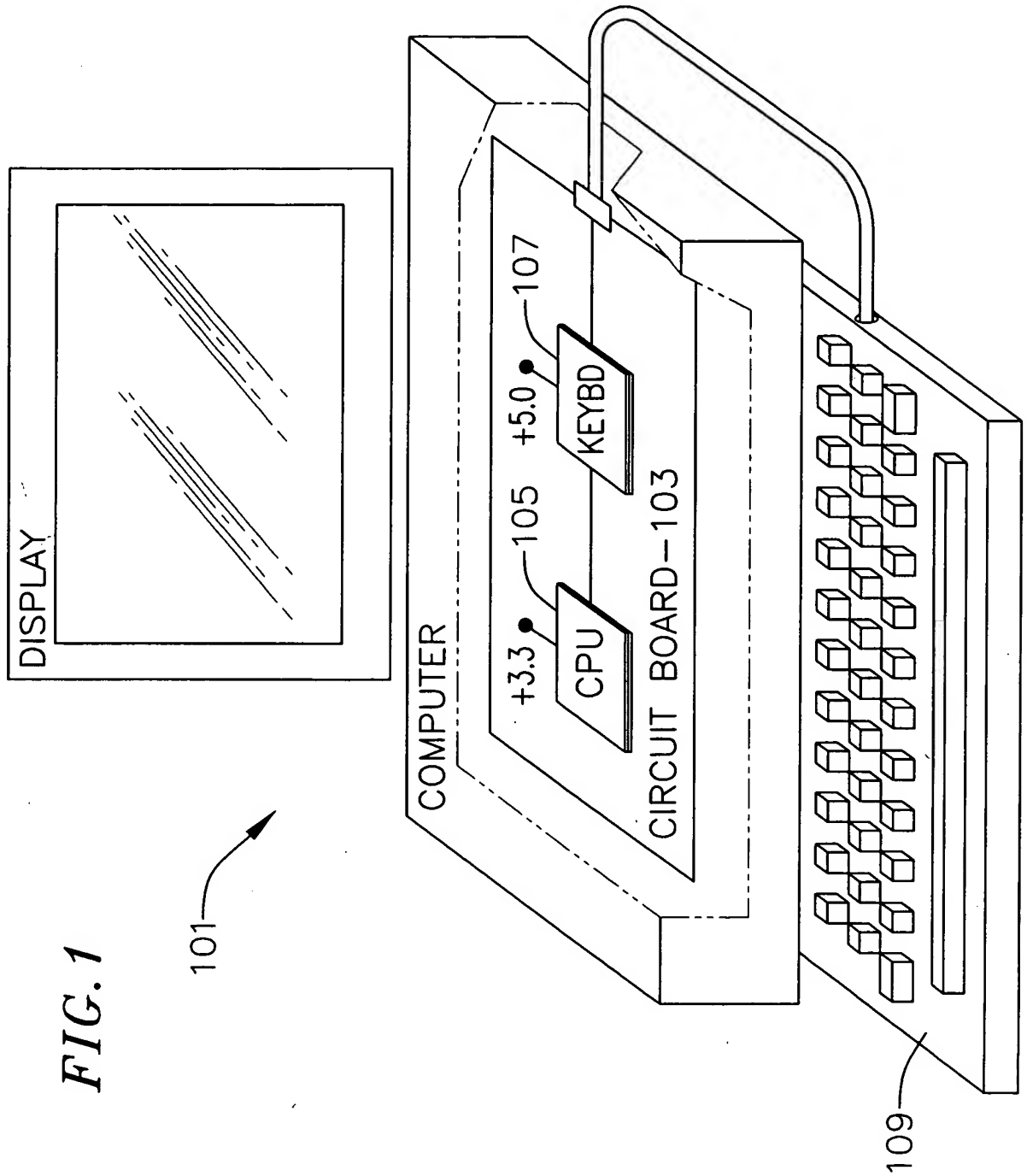


FIG. 1

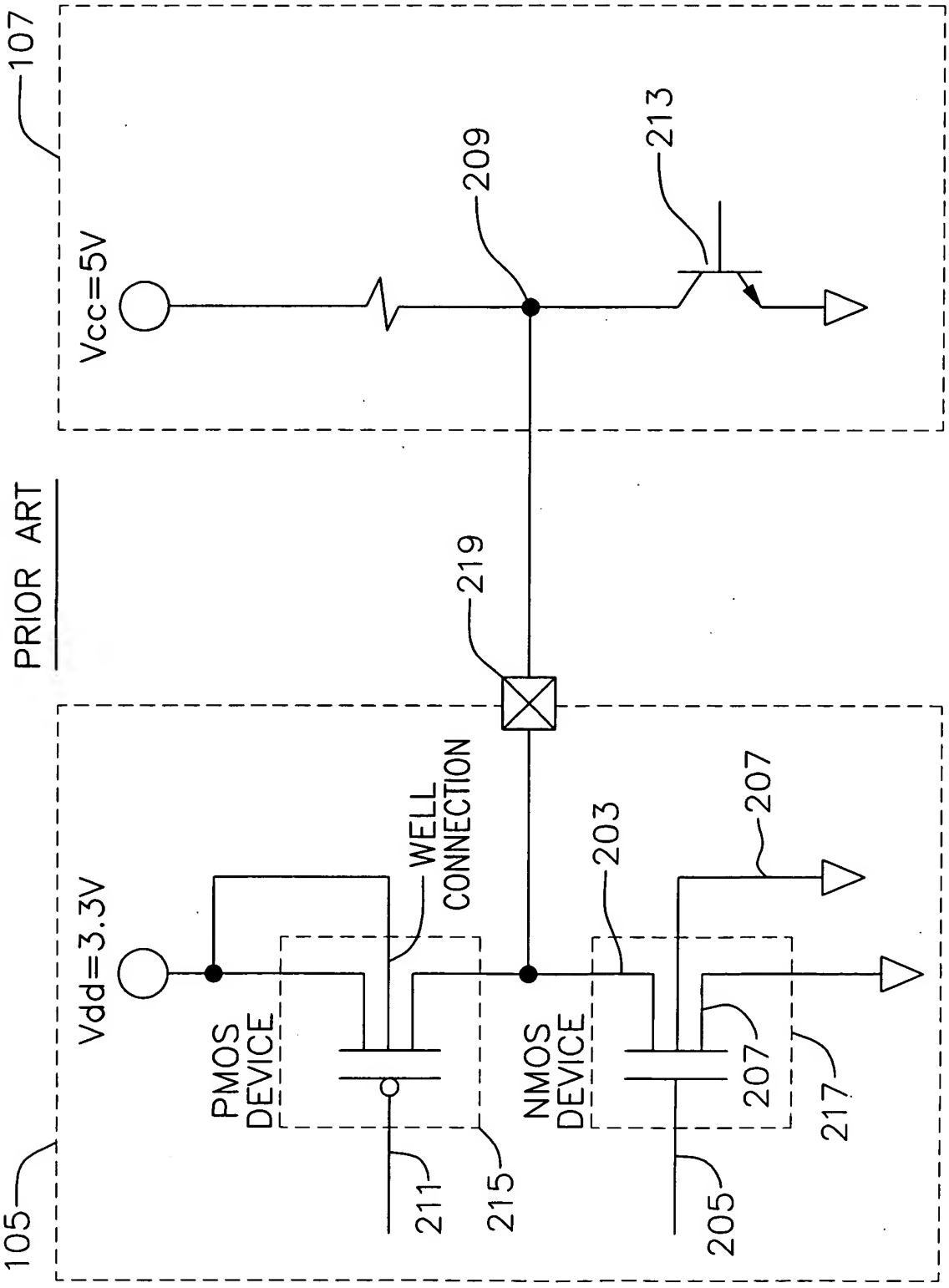


FIG.2
PRIOR ART

FIG. 3

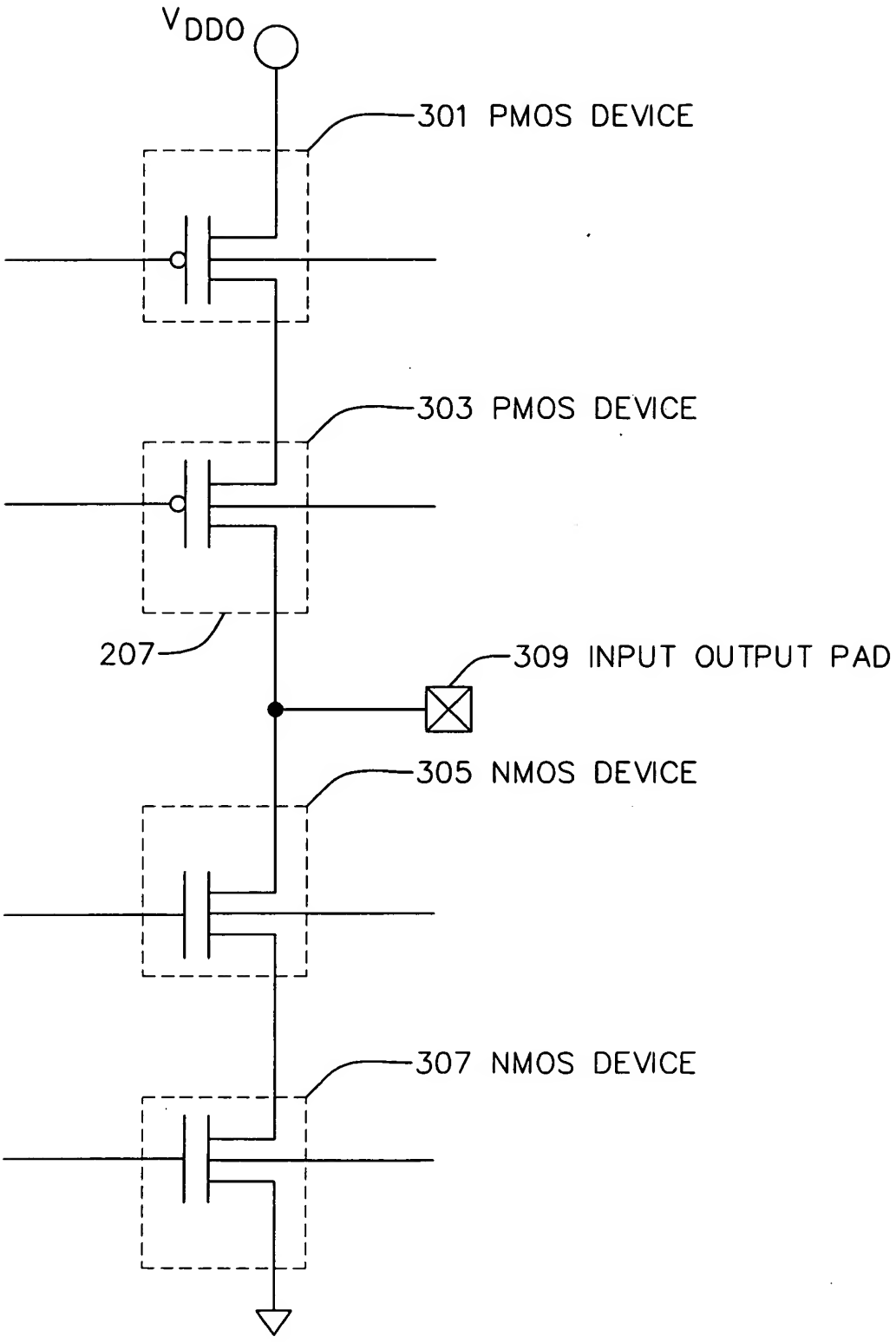

V_{DDO}
301 PMOS DEVICE
303 PMOS DEVICE
207
309 INPUT OUTPUT PAD
305 NMOS DEVICE
307 NMOS DEVICE

FIG. 4

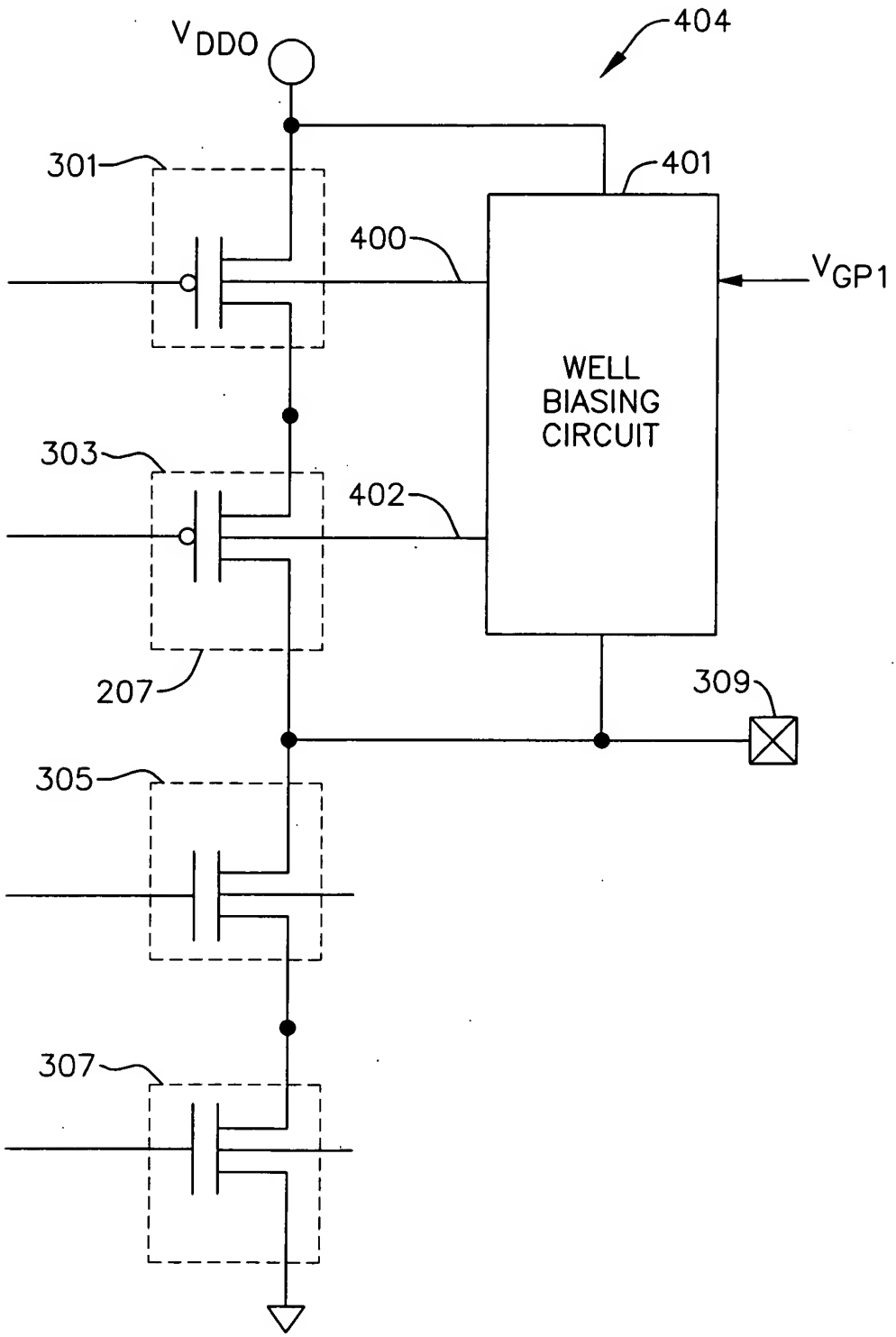

V_{DDO}
404
301
401
400
V_{GP1}
WELL BIASING CIRCUIT
303
402
207
309
305
307

FIG.5

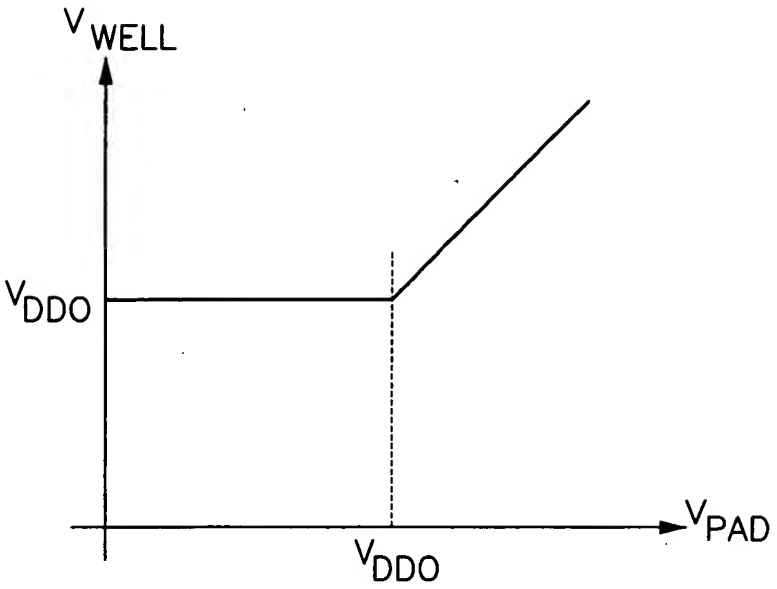


FIG. 6

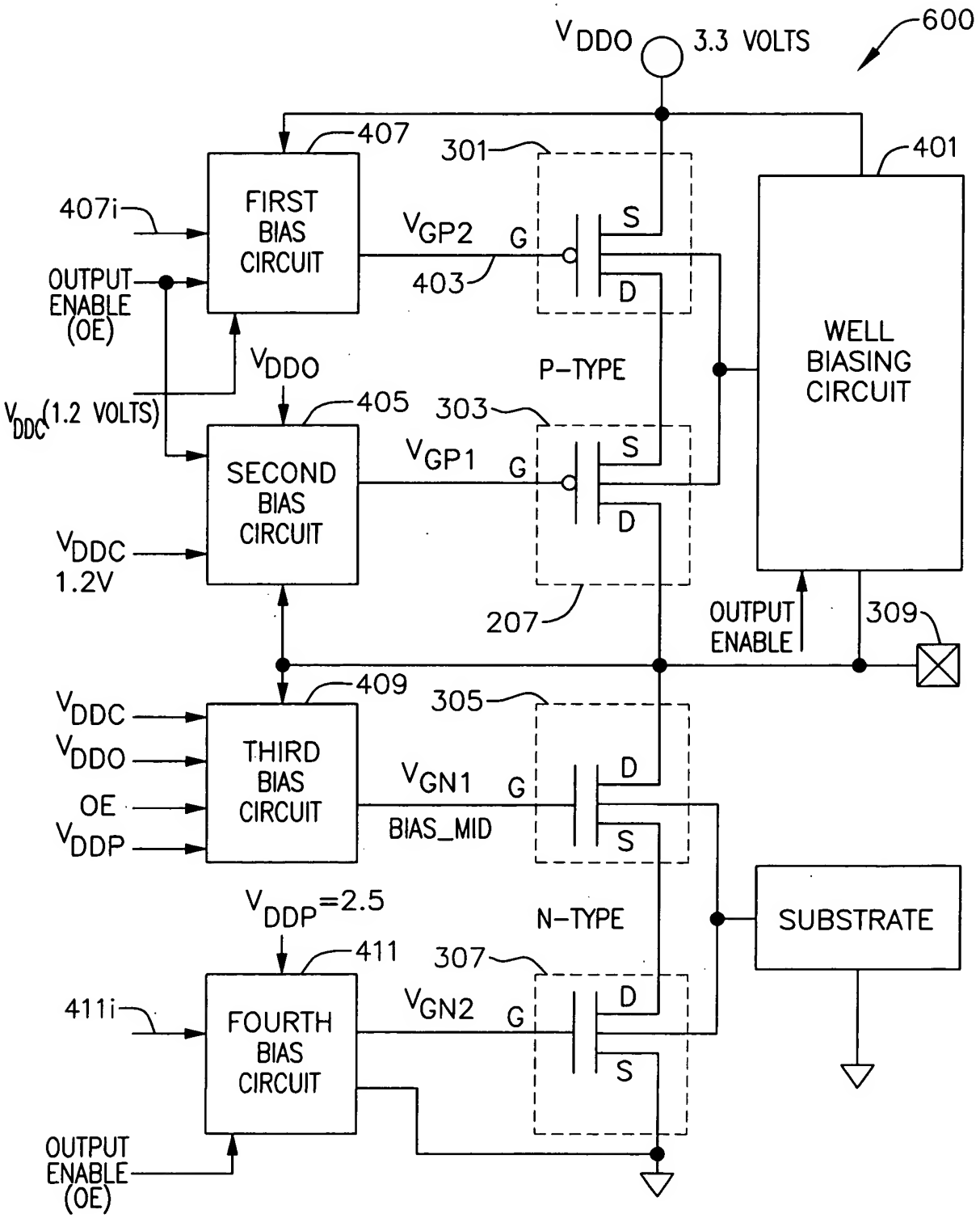

600
V_{DDO}
3.3 VOLTS
407
301
401
407i
FIRST BIAS CIRCUIT
V_{GP2}
G
S
D
403
OUTPUT ENABLE (OE)
V_{DDO}
P-TYPE
WELL BIASING CIRCUIT
V_{DDC} (1.2 VOLTS)
405
303
SECOND BIAS CIRCUIT
V_{GP1}
V_{DDC} 1.2V
207
OUTPUT ENABLE
309
409
305
V_{DDC}
V_{DDO}
OE
V_{DDP}
THIRD BIAS CIRCUIT
V_{GN1}
BIAS_MID
V_{DDP}=2.5
N-TYPE
SUBSTRATE
411
307
411i
FOURTH BIAS CIRCUIT
V_{GN2}
OUTPUT ENABLE (OE)

FIG. 7

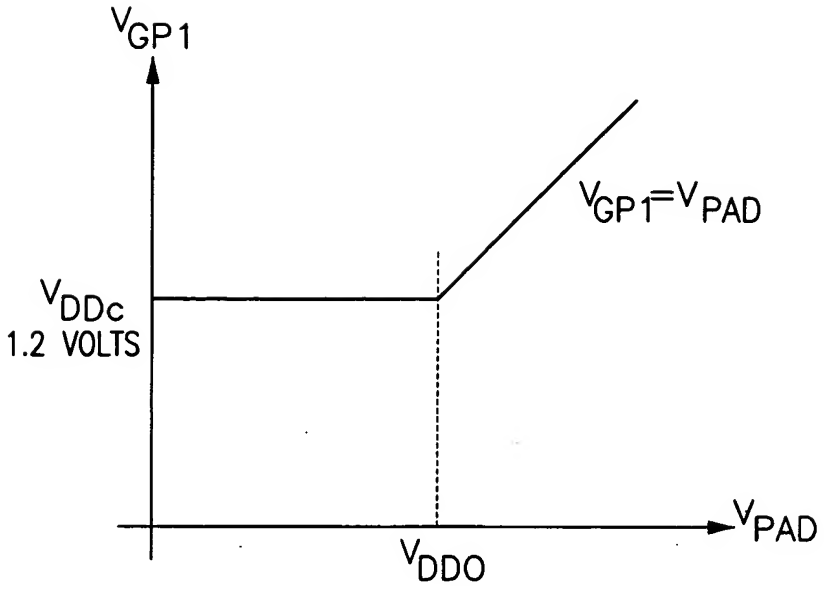
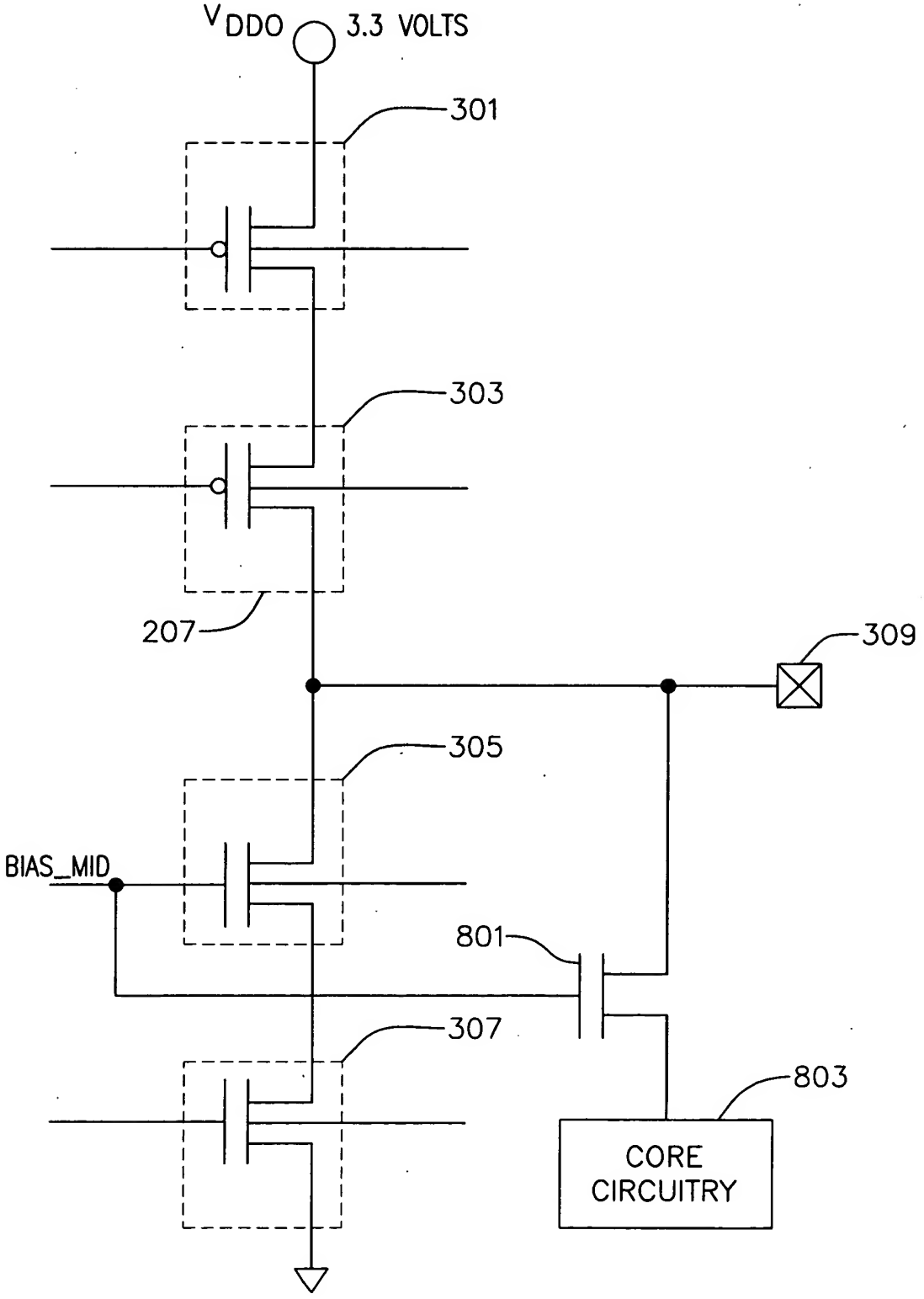


FIG. 8


VDDO
3.3 VOLTS
301
303
207
309
305
BIAS_MID
801
307
803
CORE CIRCUITRY

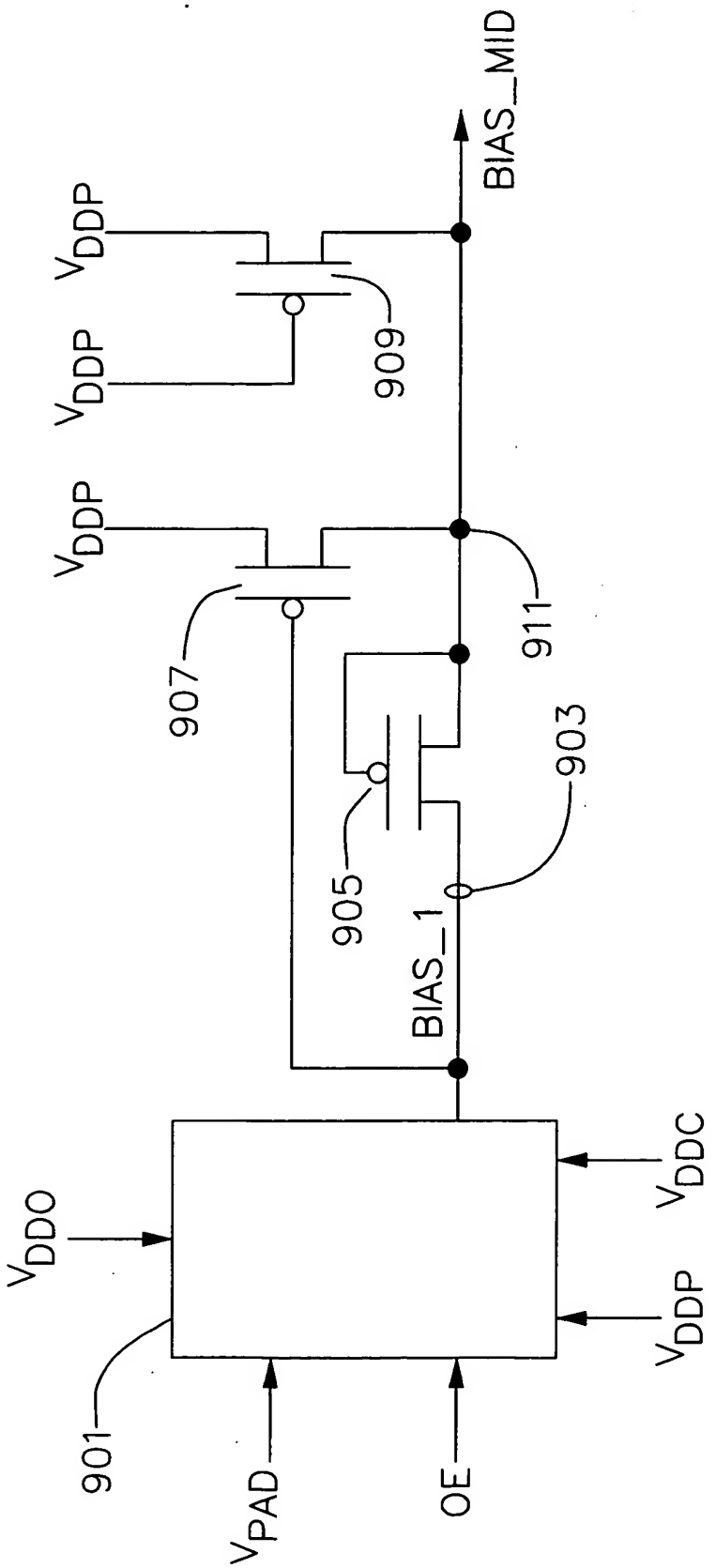

BIAS_MID
V_{DDP}
V_{DDP}
909
V_{DDP}
907
911
903
905
BIAS_1
V_{DDO}
V_{DDC}
V_{DDP}
901
V_{PAD}
OE

FIG. 9A

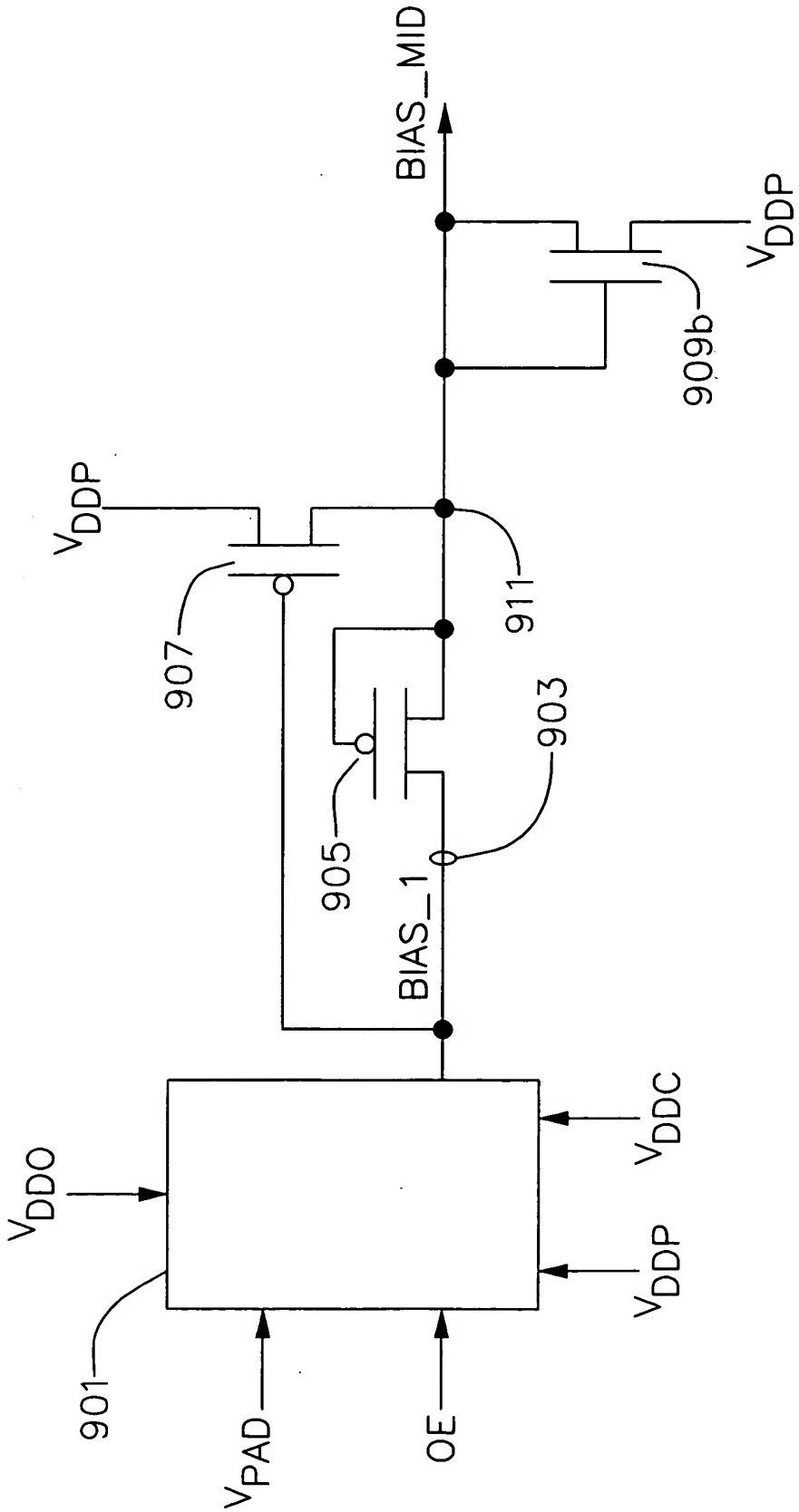

BIAS_MID
V_{DDP}
909b
V_{DDP}
907
911
903
905
BIAS_1
V_{DDO}
V_{DDC}
V_{DDP}
901
V_{PAD}
OE

FIG. 9B

FIG. 9C

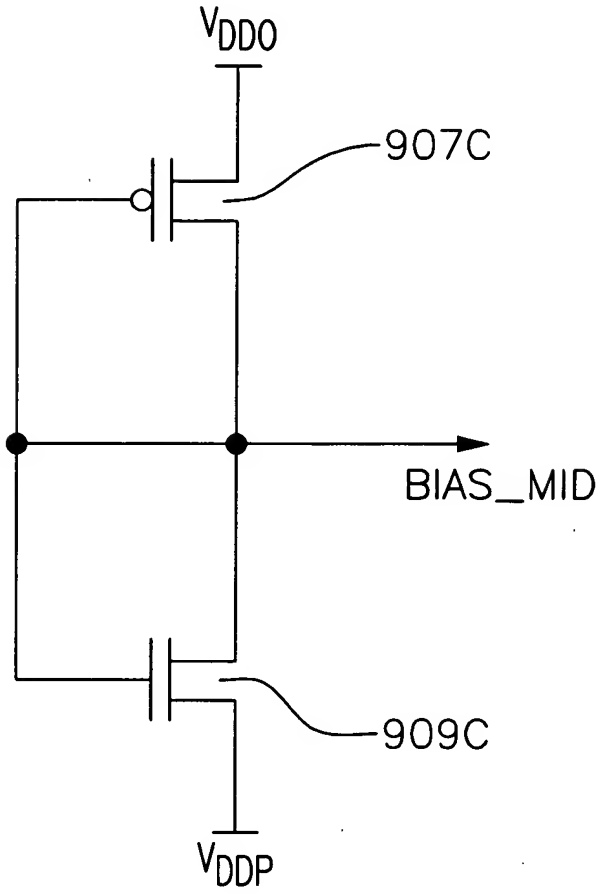


FIG. 10

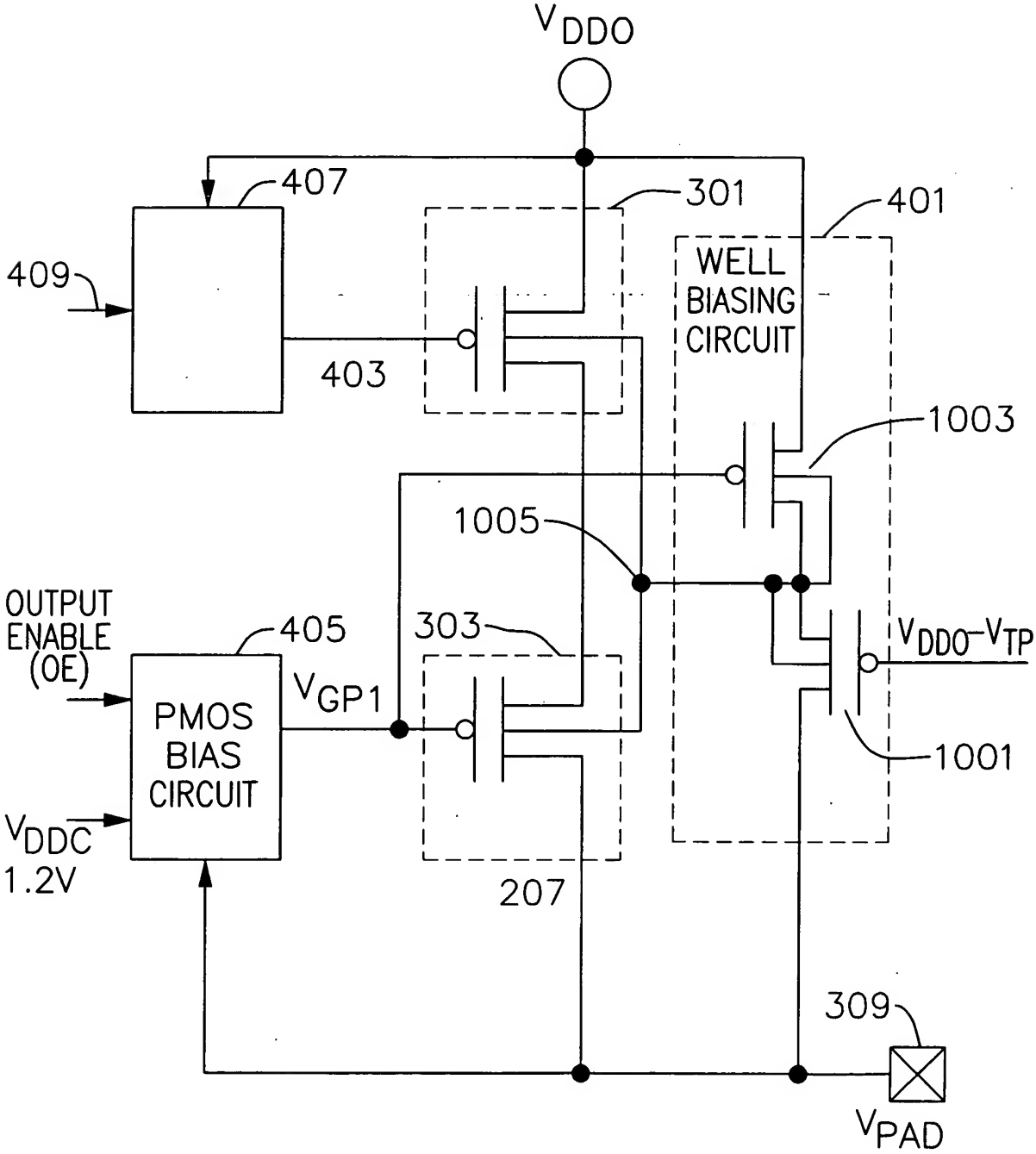

V_{DDO}
407
301
401
409
WELL BIASING CIRCUIT
403
1003
1005
OUTPUT ENABLE (OE)
405
303
$V_{DDO}-V_{TP}$
PMOS BIAS CIRCUIT
V_{GP1}
1001
V_{DDC} 1.2V
207
309
V_{PAD}

FIG. 11A

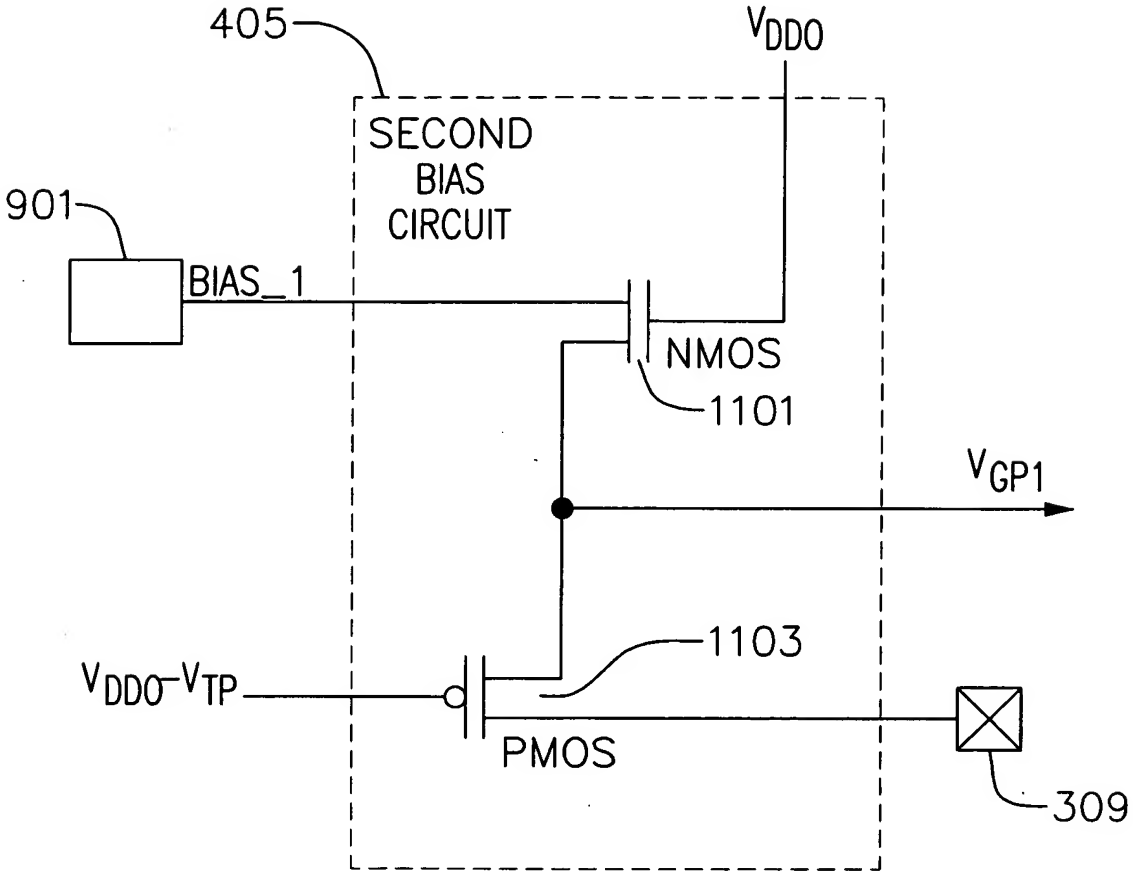

405
V_{DDO}
SECOND
BIAS
CIRCUIT
901
BIAS_1
NMOS
1101
V_{GP1}
1103
$V_{DDO}-V_{TP}$
PMOS
309

FIG. 11B

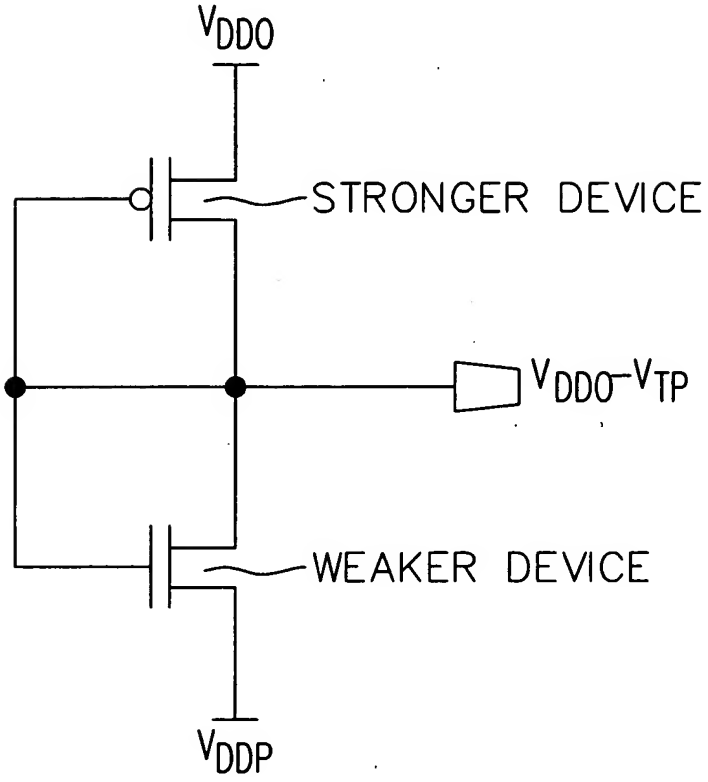


FIG. 11C

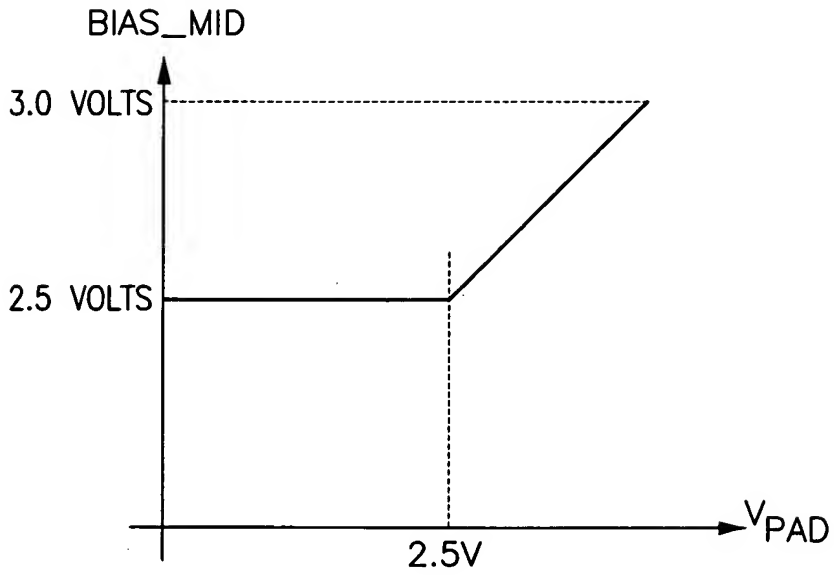
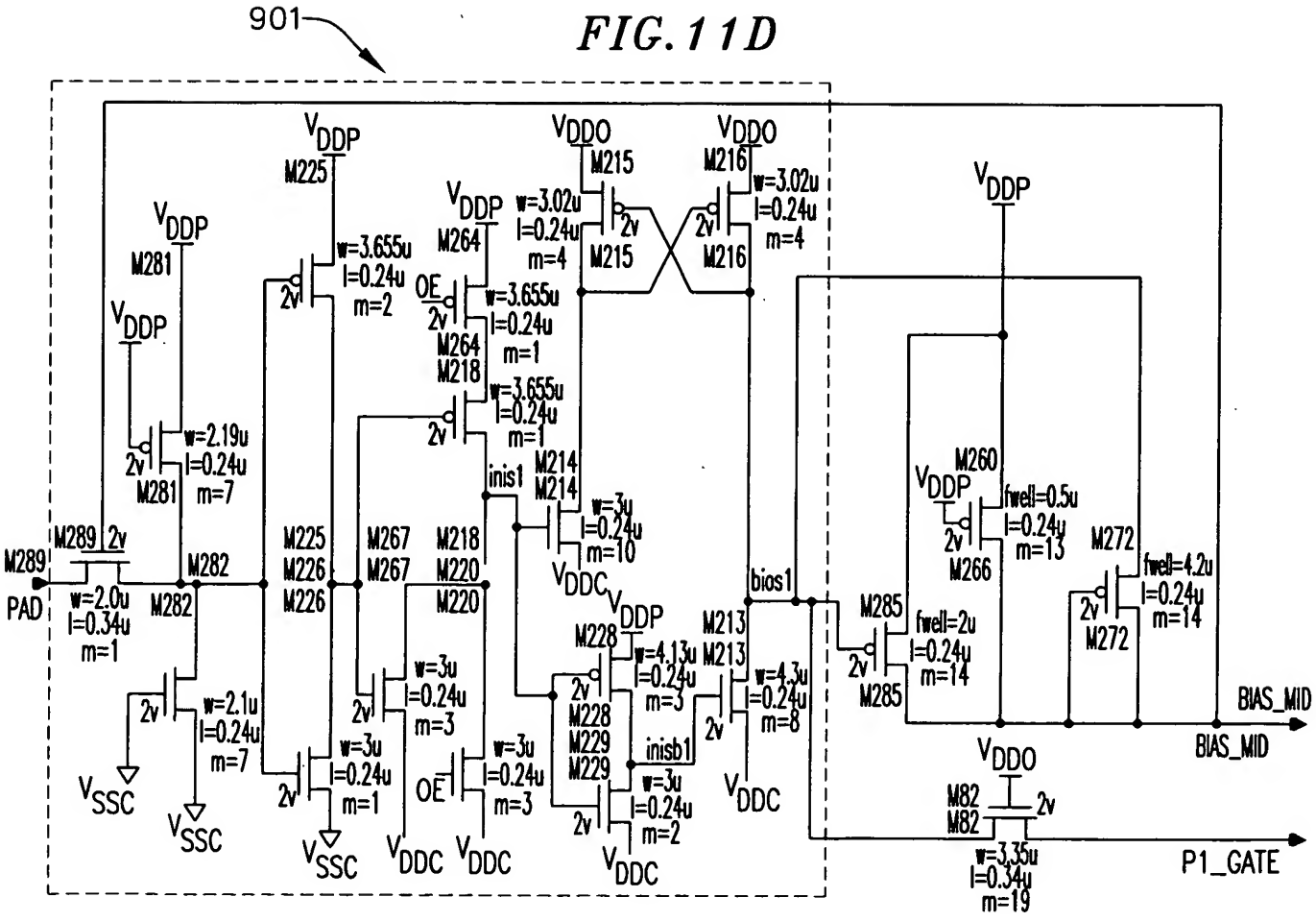


FIG. 11D


901
PAD
M289
M289 2v
w=2.0u
l=0.34u
m=1
M282
M281
V_DDP
w=2.19u
l=0.24u
m=7
w=2.1u
l=0.24u
m=7
V_SSC
M225
M226
M267
M218
M220
w=3.655u
l=0.24u
m=2
w=3u
l=0.24u
m=3
w=3u
l=0.24u
m=1
OE
M264
w=3.655u
l=0.24u
m=1
M218
inis1
M214
w=3u
l=0.24u
m=10
V_DDC
V_DDO
M215
M216
w=3.02u
l=0.24u
m=4
M228
M229
w=4.13u
l=0.24u
m=3
inisb1
w=3u
l=0.24u
m=2
M213
w=4.3u
l=0.24u
m=8
bios1
M260
fwell=0.5u
l=0.24u
m=13
M266
M285
fwell=2u
l=0.24u
m=14
M272
fwell=4.2u
l=0.24u
m=14
BIAS_MID
M82
w=3.35u
l=0.34u
m=19
P1_GATE

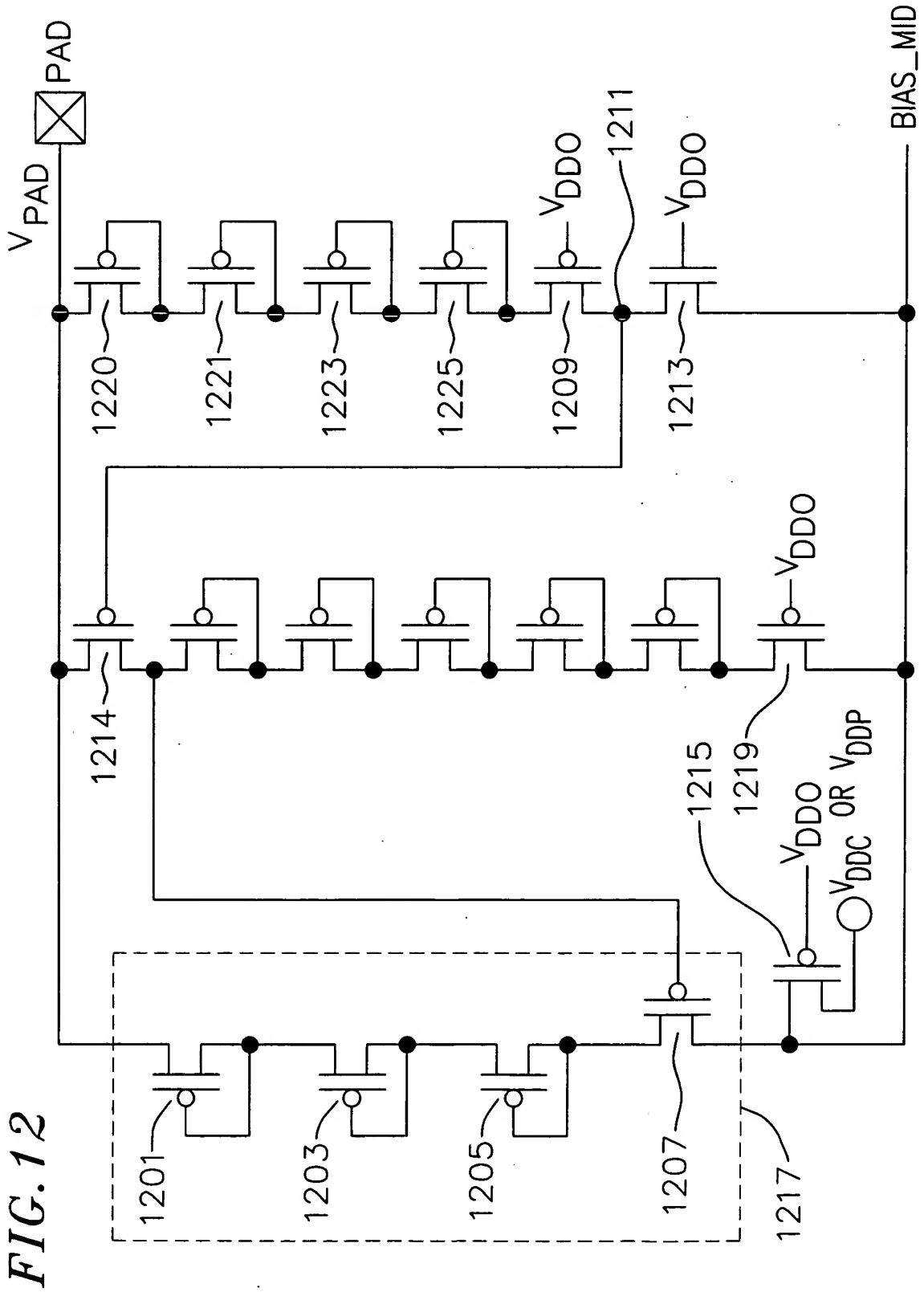
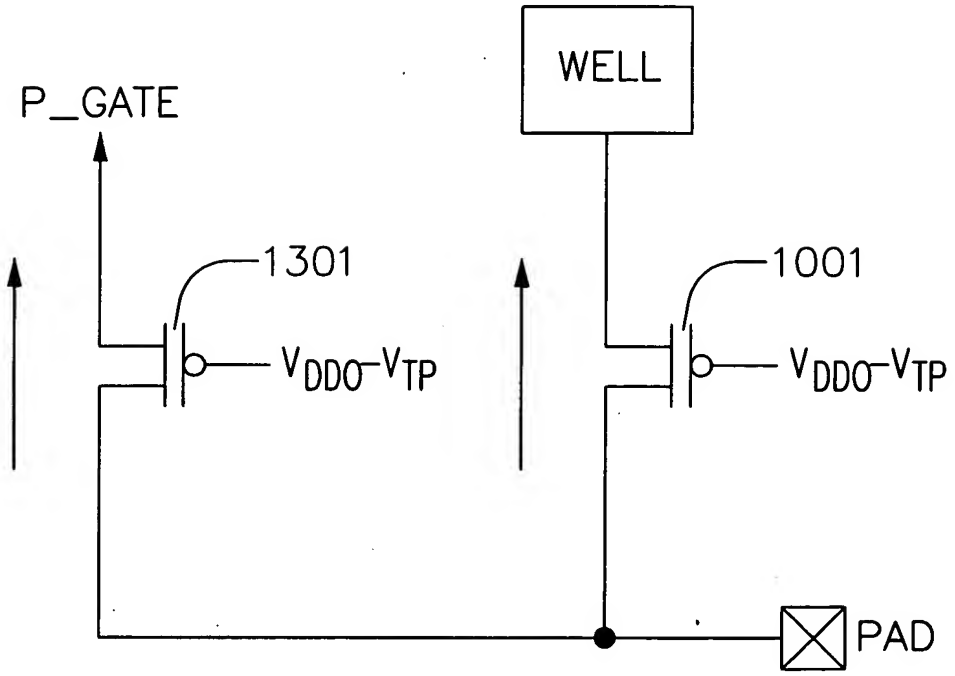

PAD
V_{PAD}
BIAS_MID
V_{DDO}
1211
1220
1221
1223
1225
1209
1213
1214
1215
1219
V_{DDO} OR V_{DDC}
V_{DDP}
1201
1203
1205
1207
1217

FIG. 12

FIG. 13



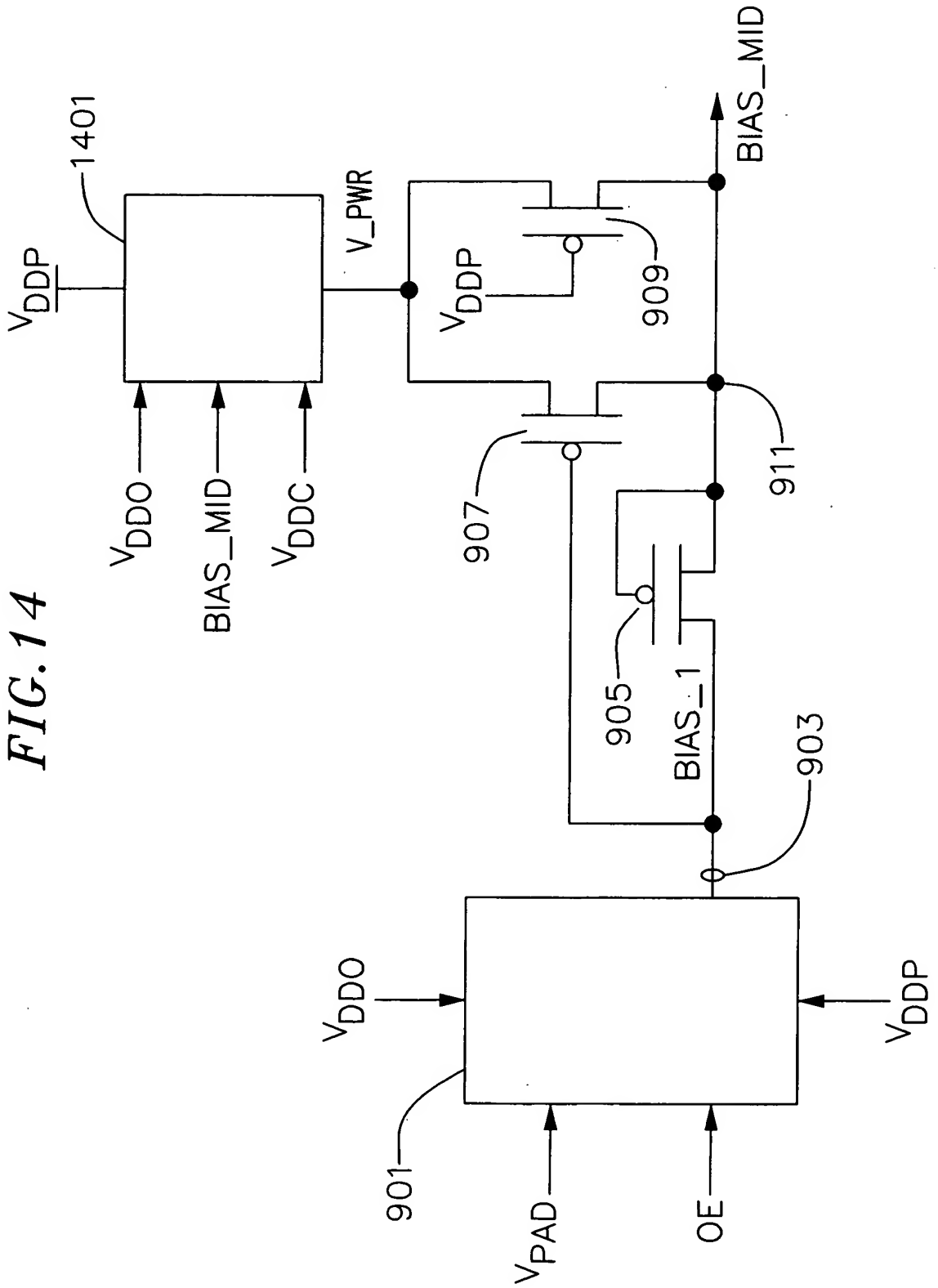

1401
V_{DDP}
V_{DDO}
BIAS_MID
V_{DDC}
V_PWR
V_{DDP}
909
BIAS_MID
907
911
905
BIAS_1
903
V_{DDO}
V_{DDP}
901
V_{PAD}
OE

FIG. 14

FIG. 15

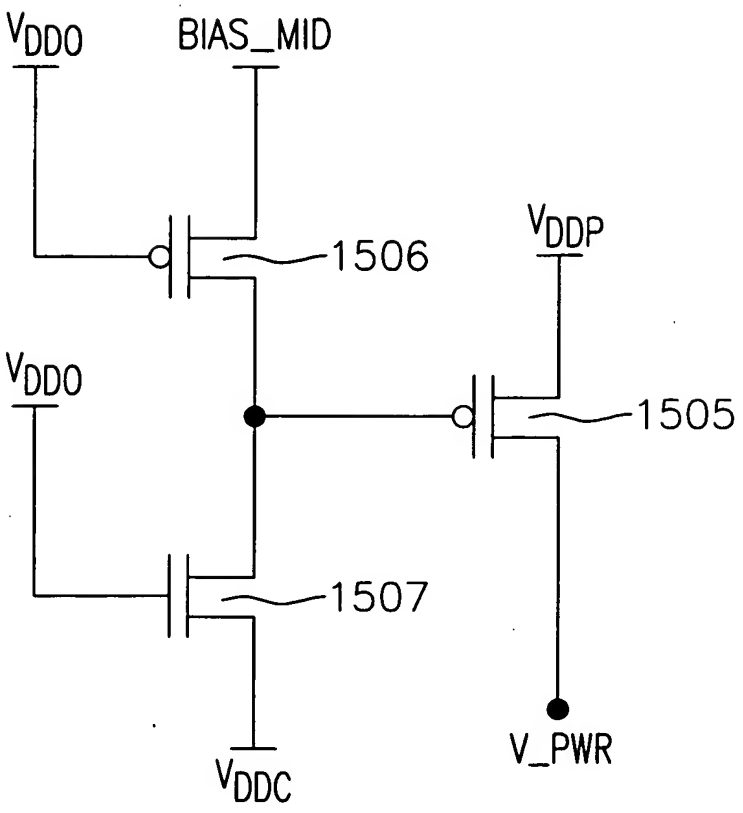


FIG. 16

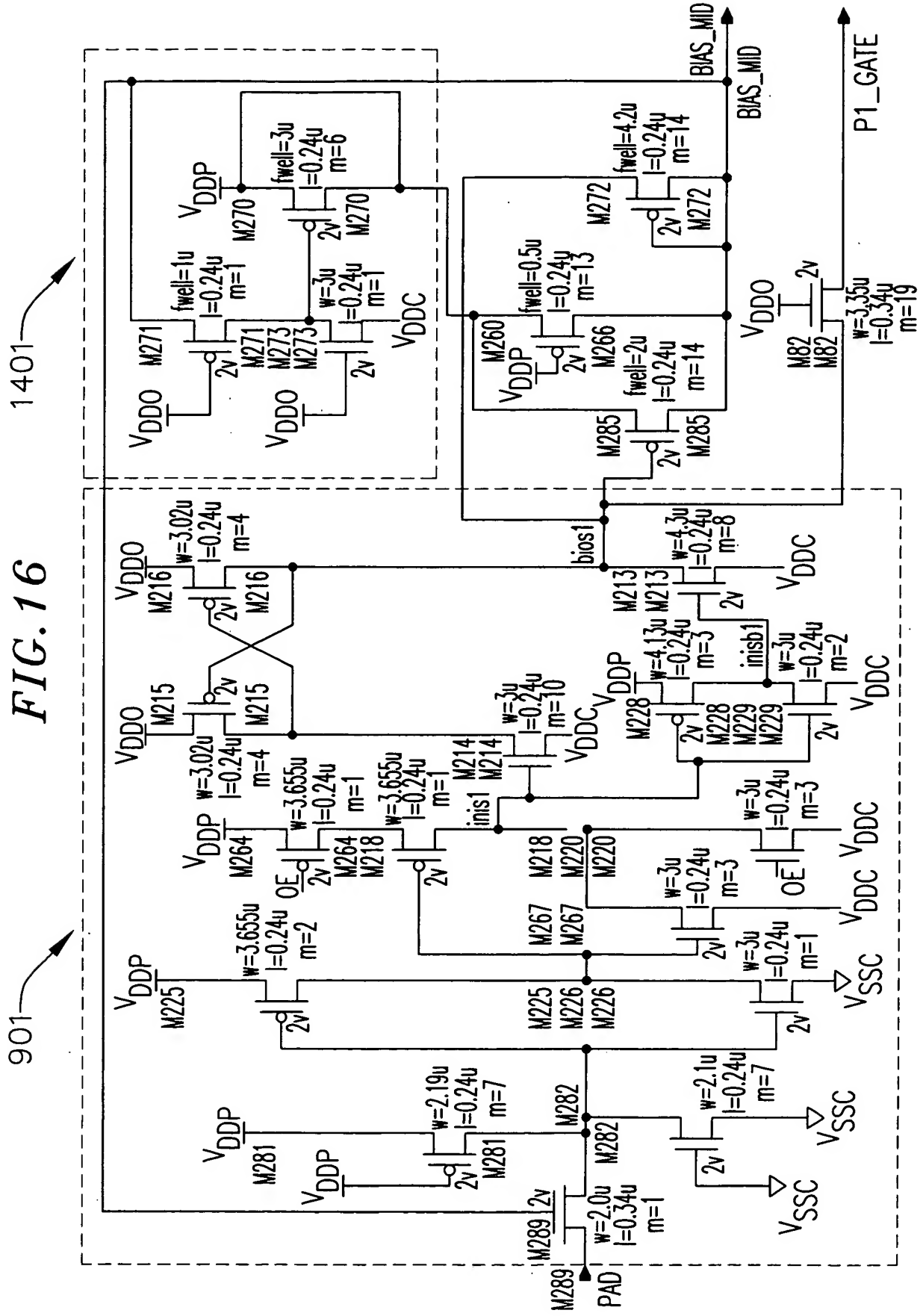

1401
901
BIAS_MID
P1_GATE
PAD
bios1
inis1
inisb1
OE
VDDO
VDDP
VDDC
VSSC
M270
M271
M273
M260
M266
M272
M285
M82
M216
M215
M213
M214
M228
M229
M264
M218
M220
M267
M225
M226
M281
M282
M289
fwell=3u
fwell=1u
fwell=0.5u
fwell=4.2u
fwell=2u
w=3u
w=3.02u
w=3.655u
w=4.3u
w=4.13u
w=2.19u
w=2.1u
w=2.0u
w=3.35u
l=0.24u
l=0.34u
m=1
m=2
m=3
m=4
m=6
m=7
m=8
m=10
m=13
m=14
m=19
2v

FIG. 17

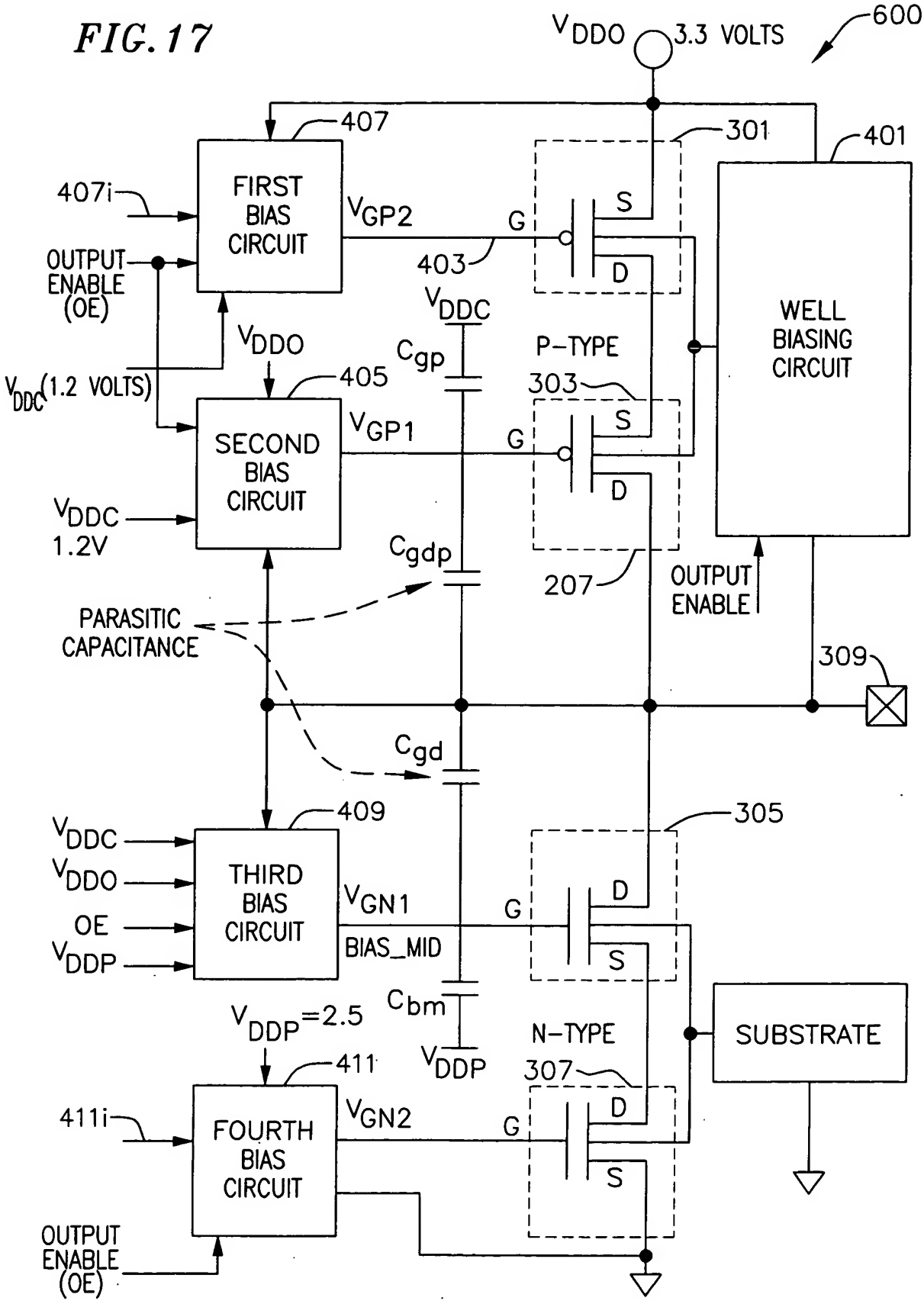
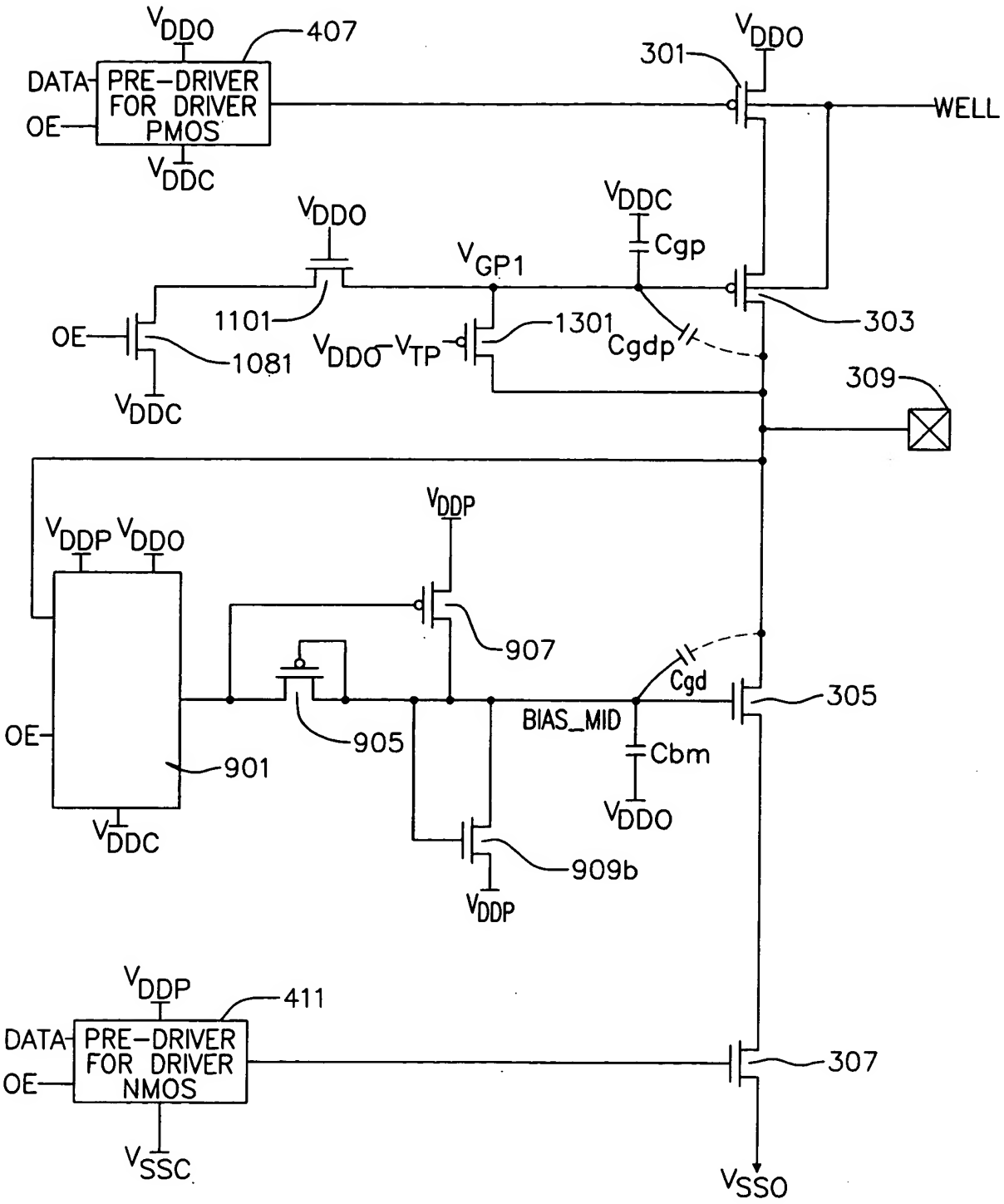

600
V_{DDO} 3.3 VOLTS
407
FIRST BIAS CIRCUIT
407i
OUTPUT ENABLE (OE)
V_{GP2}
403
301
401
S
G
D
WELL BIASING CIRCUIT
V_{DDC}
V_{DDO}
V_{DDC} (1.2 VOLTS)
C_{gp}
P-TYPE
303
405
SECOND BIAS CIRCUIT
V_{GP1}
V_{DDC} 1.2V
C_{gdp}
207
OUTPUT ENABLE
PARASITIC CAPACITANCE
309
C_{gd}
409
305
THIRD BIAS CIRCUIT
V_{DDC}
V_{DDO}
OE
V_{DDP}
V_{GN1}
BIAS_MID
C_{bm}
V_{DDP}=2.5
N-TYPE
307
411
SUBSTRATE
411i
FOURTH BIAS CIRCUIT
V_{GN2}
OUTPUT ENABLE (OE)

FIG. 18


VDDO
407
DATA
PRE-DRIVER FOR DRIVER PMOS
OE
VDDC
301
VDDO
WELL
VDDO
VGP1
VDDC
Cgp
1101
OE
1081
VDDC
VDDO VTP
1301
Cgdp
303
309
VDDP
VDDP VDDO
907
Cgd
305
OE
905
BIAS_MID
Cbm
VDDO
901
VDDC
909b
VDDP
VDDP
411
DATA
PRE-DRIVER FOR DRIVER NMOS
OE
307
VSSC
VSSO